



DVB-CID Modulator IP Core  
Specification

## Release Information

Name	DVB-CID Modulator IP Core
Version	4.0
Build date	2017.11
Ordering code	ip-dvb-cid-modulator
Specification revision	r1939

## Features

The IP core is full-featured digital DVB-CID modulator and is fully compatible with this standard:

- ETSI TS 103 129 v1.1.1 (2013-05)

## License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

## Deliverables

The DVB-CID Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

## IP Core Structure

Figure 1 shows the DVB-CID Modulator IP Core block diagram.

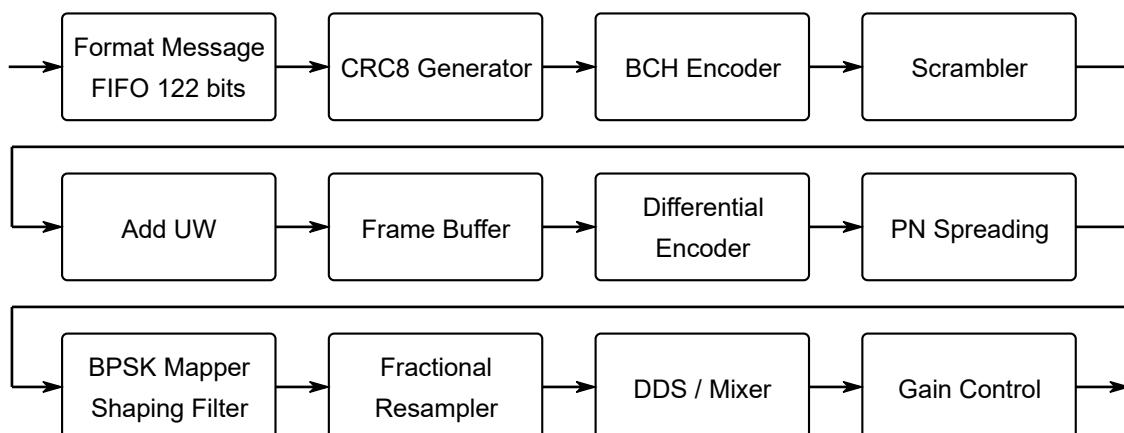
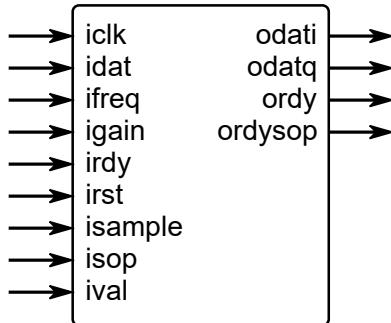


Figure 1. The DVB-CID Modulator IP Core block diagram

## Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-CID Modulator IP Core.



**Figure 2. The DVB-CID Modulator port map**

<b>Table 1. The DVB-CID Modulator port map description</b>		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	1	input (information) data
ifreq	32	output intermediate frequency
igain	16	output gain control
irdy	1	Modulator output data request.
irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	bandwidth control (symbol rate)
isop	1	input 122 bit message frame start
ival	1	input data valid
odati odatq	16	modulator complex IQ output at baseband or at intermediate frequency
ordy	1	ready to accept input data
ordysop	1	ready for start of new 122 bits frame

<b>IP Core Operation Description</b>	<p>Key features of the IP Core:</p> <ul style="list-style-type: none"> <li>• Synchronous, high-speed algorithm for the formation DVB-CID BPSK signal</li> <li>• The output of the intermediate frequency range up to 40% of the system clock frequency</li> <li>• Fractional symbol rate ratio control up to 1/4 of the system clock frequency</li> <li>• Fixed delay in modulator</li> </ul>						
<b>Setting Port Parameters</b>	<p>Some input ports that control the IP Core operation need to be set to suit custom configuration.</p>						
	<p>Carrier frequency:</p>						
	$ifreq = \frac{\text{Output Frequency (Hz)}}{\text{iclk rate (Hz)}} \cdot 2^{32}$						
	<p>Symbol rate:</p>						
	$isample = \frac{\text{Output Symbol rate (Hz)}}{\text{iclk rate (Hz)}} \cdot 2^{34}$						
	<p>Output gain:</p>						
	$igain = 8192 \cdot (10^{\frac{\text{Output gain (db)}}{20}} - 1)$						
<b>IP Core Parameters</b>	<p>Table 2 describes the DVB-CID Modulator IP Core parameters, which must be set before synthesis.</p>						
	<table border="1" data-bbox="436 1403 1357 1605"> <thead> <tr> <th colspan="2" data-bbox="436 1414 1357 1471">Table 2. The DVB-CID Modulator IP Core parameters description</th> </tr> <tr> <th data-bbox="436 1471 897 1538">Parameter</th><th data-bbox="897 1471 1357 1538">Description</th></tr> </thead> <tbody> <tr> <td data-bbox="436 1538 897 1605"></td><td data-bbox="897 1538 1357 1605">There are no parameters available to change</td></tr> </tbody> </table>	Table 2. The DVB-CID Modulator IP Core parameters description		Parameter	Description		There are no parameters available to change
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Parameter	Description						
	There are no parameters available to change						
<b>Performance and Resource Utilization</b>	<p>The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-CID Modulator IP Core measurement results.</p>						

Table 3. The DVB-CID Modulator performance

IP Core parameters	FPGA type			
	Resource	Speed grade, maximal system frequency		
Altera Cyclone V 5CEFA7	Altera Cyclone V 5CEFA7			
	1355 ALMs (3%) 1 M10K RAM blocks (1%) 12 DSP (18x18) (8%)	-8, Fmax 150.0 MHz	-7, Fmax 169.0 MHz	-6, Fmax 193.0 MHz
Xilinx Virtex-7 XC7VX330T	Xilinx Virtex-7 XC7VX330T			
	686 Slices (2%) 1 18K RAM blocks (1%) 12 DSP (18x18) (1%)	-1, Fmax 254.0 MHz	-2, Fmax 310.0 MHz	-3, Fmax 323.0 MHz

## IP Core Interface Description

Figure 3 shows the connection diagram of the DVB-CID Modulator IP Core to the existing modulator.

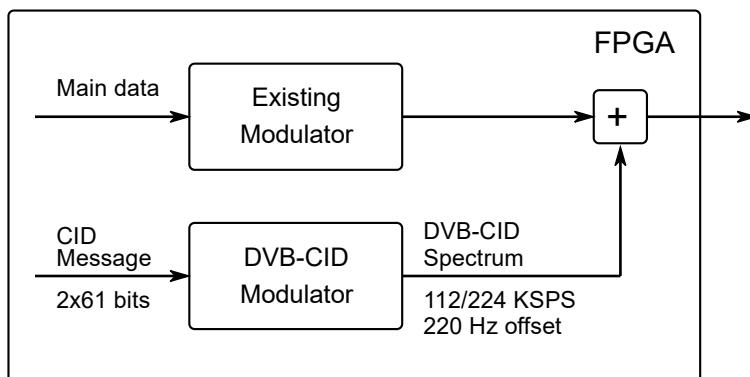
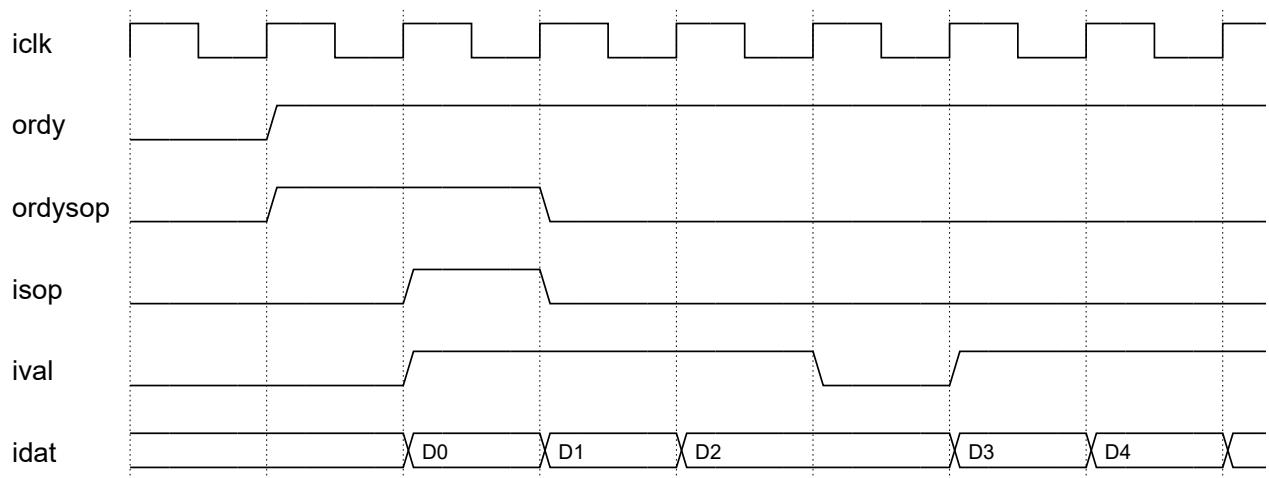


Figure 3. Connection diagram of the IP Core to the existing modulator.

Figure 4 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1"). After **ordysop** goes "1", there is 0.39 seconds to load 122 bit information frame. Each **idat** bit must be marked by **ival = 1** signal. First bit of the frame must be marked by **isop = 1** signal.



**Figure 4. The timing diagram of the IP Core input interface.**

## Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.iprium.com/ipcores/id/dvb-cid-modulator/>

## Feedback

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## Revision history

Version	Date	Changes
4.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
3.0	2014.10.21	Integrate BPSK Modulator in to the DVB-CID Modulator
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.0	2014.01.21	Official release